A METHOD OF PMOS STACKED-GATE MEMORY CELL PROGRAMMING ENHANCEMENT UTILIZING STAIR-LIKE PULSES OF CONTROL GATE VOLTAGE

Inventors: Yuri Mirgorodski, Sunnyvale, California
Vladislav Vashchenko, Palo Alto, California
Peter J. Hopper, San Jose, California

TECHNICAL FIELD

The present invention is directed to a method of programming a PMOS stacked-gate memory cell by a hot electron injection mechanism that utilizes a sequence of stair-like pulses of control gate voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a partial cross-section drawing illustrating the general structure of a PMOS stacked gate memory cell.

Fig. 2 is a graph showing PMOS device floating gate current versus floating gate voltage.

Fig. 3 is a graph showing PMOS device control gate voltage, drain voltage and Vt shift versus time.

DESCRIPTION OF THE INVENTION

Hot electron injection is a well-known and widely used method of programming non-volatile memory (NVM) cells. It is a common programming mechanism for stacked-gate cells, split-gate cells and other currently available NVM cells.

Fig. 1 provides a general schematic representation of a conventional PMOS stacked gate NVM cell 100 formed in an N-type region 102 of semiconductor material, e.g. crystalline silicon. Those skilled in the art will appreciate that the N-type region 102 is typically an n-well formed in a P-type silicon substrate. The PMOS device 100 includes a conductive floating gate (FG) electrode 104, e.g. polysilicon, that is separated from the N-type region 102 by a layer of thin gate dielectric material 106, e.g. silicon dioxide. A control gate (CG) electrode 108, e.g. polysilicon, is separated from the floating gate 104 by a layer of

intergate dielectric material 110, e.g. an oxide-nitride-oxide (ONO) sandwich. P-type diffusion regions 112 formed at the sides of the stacked gate structure provide the source/drain regions of the PMOS cell 100 and define an N-type channel region therebetween. The fabrication techniques available for making the PMOS device 100 are well known.

When applied to a PMOS based stacked-gate cell 100, the hot electron injection programming method assumes that a high negative voltage is applied to the drain of the PMOS device. Depending on the erasing and coupling coefficient, a corresponding voltage is applied to control gate 108 that brings the potential of the floating gate 104 to a value that is negative, but lower in absolute value compared with drain. In these conditions, the high lateral electric field creates hot electrons, and the high perpendicular electric field helps the hot electrons to reach the floating gate 104 through the thin gate oxide 106. The injection current essentially depends on the potential of the drain and the floating gate 104; that is, the more drain voltage, the more injection.

As shown in the Fig. 2 graph of PMOS gate current versus floating gate voltage, the gate current of the PMOS device 100 has a maximum with respect to the floating gate 104 voltage.

With continuing reference to the Fig. 2 graph, traditional programming starts from a floating gate potential that is close to the right side of the pick, i.e. position 1 on the Fig. 2 graph. During programming, the floating gate 104 receives a negative charge of electron injection current. As a result, the floating gate potential moves to more negative values until it stops in a position 2 on the Fig. 2 graph with very low injection current. This means the end of programming that results in a shift of the threshold voltage V_t of the PMOS device 100 that is equal to the voltage difference (Delta) between position 1 and position 2 on the Fig. 2 graph. This shift depends on the drain voltage via the pick's width; it does not depend on pick's height. The control gate voltage only gives a start to the programming, but does not affect V_t shift.

In accordance with the present invention, the conventional hot electron injection programming procedure is repeated, each repetition bringing the floating gate potential back to the position 1 in Fig. 2 by means of a sequence of control gate pulses, as shown in Fig. 3.

The control gate pulse step up and the frequency of the pulse repetitions are important. Steps that are either too small or too large will not improve programming. In accordance with the invention, and as shown in Fig. 3, the control gate voltage pulses should have a step up that is approximately equal to Delta divided by the coupling coefficient. The time between pulses should be long enough to allow the floating gate to come to the position 2.

This method allows the programming effect to be increased by increasing only the control gate voltage with no increase in drain voltage/current. The method also offers a decrease of drain voltage/current without decreasing the programming effect.

As further shown in Fig. 3, because the control gate voltage in the programming regime is normally negative, the first few steps up do not result in any increase of supply voltage. If the control gate voltage rises to positive values, it becomes necessary to increase the supply voltage.

In accordance with the concepts of the invention, a corresponding delay circuit can be provided that produces an optimal control gate voltage increase during the programming operation. Thus, the shape of the control gate voltage pulse can be measured and implemented according to process development results or using laser trimming.

Although only specific embodiments of the present invention are shown and described herein, the invention is not to be limited by these embodiments. Rather, the scope of the invention is to be defined by these descriptions taken together with the attached claims and their equivalents.